

### **Amendments to the Specification**

*In the Abstract, please amend the following. This amendment was requested in the response filed on July 14, 2007. Present here again for Examiner's convenience. Separate page for Abstract follows Remarks/Arguments.*

Test stimulus data is shifted into a first module 3A, and test response data captured in response to a global scan enable signal 27 being activated. Each module comprises a control circuit 59A, 59B, for example an OR gate, for controlling whether or not the global scan enable signal 27 is passed to its respective module. The control circuits 59A, 59B are controlled by a dedicated bypass signal 61A, 61B, respectively. The dedicated bypass signals 61A, 61B act as control signals for controlling whether or not the local scan enable signals 60A and 60B mirror the global scan enable signal 27. This enables the global scan enable signal 27 to be kept high for one or more particular modules that are not being tested, by maintaining the dedicated bypass signal 61A or 61B high for those particular modules, such that they are placed in a transport mode of operation. The invention allows test pattern data to be processed in a pipelined manner, such that modules located prior to the module being tested contain the next set of test stimulus data from a series of test stimulus data, and modules located after the module to be tested contain test response data from previous tests.

According to an example embodiment of the present invention, there is a test access architecture for testing modules in an electronic circuit. The test access architecture includes a test access mechanism (TAM) having a plurality of modules connected in series thereto; the test access mechanism is arranged to transport test stimulus data to, and test response data from a module being tested. A global enable signal is provided for placing the modules in a test mode. A control circuit is provided between the global enable signal and an associated module; wherein the control circuit is arranged to control whether or not the global enable signal is passed to its associated module.